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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,064	03/16/2004	Ho-Ouk Lee	8750-064	5182

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EXAMINER	
QUACH, TUAN N	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 09/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/803,064	LEE ET AL.	
	Examiner	Art Unit	
	Tuan Quach	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-21* is/are pending in the application.

4a) Of the above claim(s) *21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10,13-16* is/are rejected.

7)☒ Claim(s) *11,12 and 17-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This application contains claims directed to the following patentably distinct species of the claimed invention:

1. The species of claims 10-20 corresponding to a method of manufacturing a semiconductor device, comprising: preparing a semiconductor device having a cell array region and a peripheral circuit, region; sequentially forming a gate insulating layer and a gate conductive layer on the semiconductor substrate; forming a word line capping layer and a gate capping layer on the gate conductive layer; patterning the word line capping layer the gate capping layer and the gate conductive layer to form a plurality of word line patterns in the cell array region and al least one gate pattern in the peripheral circuit region the word line pattern including a word line and a word line capping layer pattern, the gate pattern including a gate electrode and a gate capping layer pattern, forming gate spacers on side walls of the word line pattern and the gate pattern, sequentially forming a pad interlayer insulating layer and a bit line interlayer, insulating layer over a surface of the semiconductor substrate having the gate spacers, patterning the bit line interlayer insulating layer, the pad interlayer insulating layer and the gate capping layer pattern to form a cell contact hole penetrating a region between the word line patterns and a peripheral circuit contact hole exposing the gate electrode.

2. The species of the claimed invention in claim 21 regarding a method comprising forming a gate insulating layer on a cell array region and a peripheral circuit region of a substrate; forming a gate conductive layer on the gate insulating layer; forming a word line capping layer on the gate conductive layer; etching the word line capping layer to expose the gate conductive layer in the peripheral circuit region; forming a gate capping layer on the word line capping layer in the cell array region and on the gate conductive layer in the peripheral circuit region; planarizing the gate capping layer in the cell array region to expose the word line capping layer; patterning the word line capping layer, the gate conductive layer, and the gate insulating layer in the cell array region to form word line patterns, the word line patterns having sidewalls; patterning the gate capping layer the gate conductive layer, and the gate insulating layer in the peripheral circuit region to form at least one gate pattern the at least one gate pattern having sidewalls; forming gate spacers on the sidewalls of the word line patterns and the at least one gate pattern; forming a pad interlayer insulating layer that covers the word line patterns and the at least one gate pattern forming a bit line interlayer insulating layer on the pad insulating layer; patterning the bit line interlayer insulating layer and the pad insulating layer to form a cell contact hole exposes a portion of the substrate between the word line patterns; and pattterning the bit line interlayer insulating layer, the pad insulating layer, and the gate capping layer to form a peripheral circuit contact hole that exposes the gate conductive layer in the at least one gate pattern.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, no claim is generic.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

Newly submitted claim 21 directed to an invention that is independent or distinct from the invention originally claimed for the reasons delineated above.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claim 21 is withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 10, 15 rejected under 35 U.S.C. 102(b) as being anticipated by Ha (6,451,708).

Ha teaches all the claimed process steps of claim 10, including a method of preparing a semiconductor device having a cell array region and a peripheral circuit

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Claims 13, 14, 16 are rejected under 35 U.S.C. 103(a) as being obvious over Ha supra.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Claims 13, 14, 16 are rejected under 35 U.S.C. 103(a) as being obvious over Ha supra.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned

by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Regarding claim 13, the etching the capping layers and of the conductive layer using the capping layer pattern as mask is taught also, column 5 lines 20 seq.; although the simultaneous language is not explicitly recited such would have bee obvious and/or encompassed therein as the conductive layers are patterned to form the stacks in question and wherein simultaneous patterning or separately patterning correspond to two obvious expedients to form the patterns as in claims 13 and 14. Regarding claim 16, the intended use of self-align does not require any additional structure or processing and would have been obvious or inherent or encompassed in the processing as previously delineated and therefore unpatentable thereover; alternatively, it would have been obvious where alignment is not employed or required or unnecessary with existing structures or components.

Claims 11, 12, 17-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims as previously indicated.

As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Applicant's arguments filed June 23, 2005 have been fully considered but they are not persuasive.

Regarding claims 10 and 15, applicant argues that Ha does not teach the gate capping layer, the patterning to form the word line patterns and the gate pattern. The argument does not appear to take into the teachings of Ha as delineated above. In particular, Ha teaches all the claimed process steps of claim 10, including a method of preparing a semiconductor device having a cell array region and a peripheral circuit region, sequentially forming a gate insulating layer 106 and a gate conductive layer 108 on the semiconductor substrate 100, forming a word line capping layer 110 and a gate capping layer on the gate conductive layer, patterning the word line capping layer, the gate capping layer, and the gate conductive layer to form a plurality of word line patterns in the cell array region and at least one gate pattern in the peripheral region, the word line pattern including a word line and a word line capping pattern, the gate pattern including a gate electrode and a gate capping layer pattern, forming gate spacers 112 on the side walls of the word line pattern and the gate pattern, sequentially forming a pad interlayer insulating layer 118 and a bit line interlayer insulating layer 120 over a surface of the semiconductor substrate having the gate spacers; and patterning the bit line interlayer insulating layer, the pad interlayer insulating layer, and the gate capping layer pattern to from a cell contact hole 126 penetrating a region between the word line patterns and a peripheral circuit contact hole 124 exposing the gate electrode. See Figs. 2A-2F, column 4 line 66 to column 7 line 18. Compare for instance, instant figures with Figs. 2A-2F and the corresponding teachings delineated above wherein the gate capping patterning is readily apparent to one skilled in the art.

Regarding claims 13, 14, 16, applicant further argues that Ha fails to establish prima facie obviousness. Nonetheless, applicant fails to consider regarding claim 13, the etching the capping layers and of the conductive layer using the capping layer pattern as mask is taught also, column 5 lines 20 seq. It remains apparent that although the simultaneous language is not explicitly recited such would have bee obvious and/or encompassed therein as the conductive layers are patterned to form the stacks in question and wherein simultaneous patterning or separately patterning correspond to two obvious expedients to form the patterns as in claims 13 and 14. Regarding claim 16, the intended use of self-align does not require any additional structure or processing and would have been obvious or inherent or encompassed in the processing as previously delineated and therefore unpatentable thereover; alternatively, it would have been obvious where alignment is not employed or required or unnecessary with existing structures or components. It remains apparent that such does not require any inventiveness and would have been obvious over Ha which applicant has failed to rebut.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Tuan Quach whose telephone number is 571-272-1717. The examiner can normally be reached on M-F from 8:30 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Nathan Flynn, can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan Quach
Primary Examiner